CHEMICAL MECHANICAL PLANAR TODAY

Planarization process becoming method of choice despite manufacturing, cost issues

by Katherine Derbyshire

MAKING CMP WORK

When it first appeared on the scene, process engineers greeted chemical mechanical planarization (CMP) with shock and derision. Mechanical grinding with a particle-laden slurry, mere microns away from the wafer's exquisitely polished surface, was nothing short of heresy. Fab managers who had religiously shunned every possible particle source now had to tolerate unimaginable levels of filth. Just a few short years later, CMP now contributes to every layer, from transistor fabrication to final metallization.

Chemical mechanical planarization first entered semiconductor manufacturing as a way to reduce topography on the wafer. Multilevel metallization schemes reproduce "up" areas and "down" areas from one level to the next. Each metal layer magnifies topography from the layer below it, while adding more features of its own. As shrinking feature sizes required higher numerical apertures for lithography and the number of metal layers increased, these topographic variations exceeded the available depth-of-focus budget. CMP flattens out the peaks, thus creating a flat surface that allows consistent focus across the entire exposure field.

The oxide CMP process used for this first application is mature now. Fabs can expect consistent yield within an acceptable process window. However, most other CMP steps are further back along the learning curve, and that's where the action is.

CMP FOR DAMASCENE INTERCONNECTS

Damascene interconnect schemes could not exist without CMP or a similar planarization method. Conventional interconnect schemes begin with a blanket layer of the conductor, usually aluminum. A patterning step cuts trenches, which are then filled with dielectric, usually silicon dioxide (SiO_2). This subtractive metallization has served the industry well for 30 years.

Copper, however, is very difficult to etch. Most possible plasma chemistries form nonvolatile reaction products that remain on the wafer. Damascene interconnect schemes accommodate this behavior by cutting trenches into a blanket dielectric instead, then filling those trenches with metal. For copper interconnects, the fill process includes a diffusion barrier, a copper seed layer, and electrochemical deposition for the bulk fill. The final step uses CMP to polish the excess metal away, leaving a flat surface for the next dielectric layer.

The article "Copper Interconnects Face Fab Realities" in the November 2001 issue of *Semiconductor Magazine*, discussed copper integration issues in

continued on page 42